

IS61NLP6432A

IS61NLP6436A/IS61NVP6436A

IS61NLP12818A/IS61NVP12818A



64K x 32, 64K x 36, and 128K x 18 2Mb, PIPELINE 'NO WAIT' STATE BUS SRAM

PRELIMINARY INFORMATION
SEPTEMBER 2005

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/W (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Power Down mode
- Common data inputs and data outputs
- $\overline{\text{CKE}}$ pin to enable clock and suspend operation
- JEDEC 100-pin TQFP package
- Power supply:
NVP: V_{DD} 2.5V ($\pm 5\%$), V_{DDQ} 2.5V ($\pm 5\%$)
NLP: V_{DD} 3.3V ($\pm 5\%$), V_{DDQ} 3.3V/2.5V ($\pm 5\%$)
- Industrial temperature available
- Lead-free available

DESCRIPTION

The 2 Meg 'NLP/NVP' product family feature high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for networking and communications applications. They are organized as 64K words by 32 bits, 64K words by 36 bits, and 128K words by 18 bits, fabricated with ISSI's advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{\text{CKE}}$ is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when $\overline{\text{WE}}$ is LOW. Separate byte enables allow individual bytes to be written.

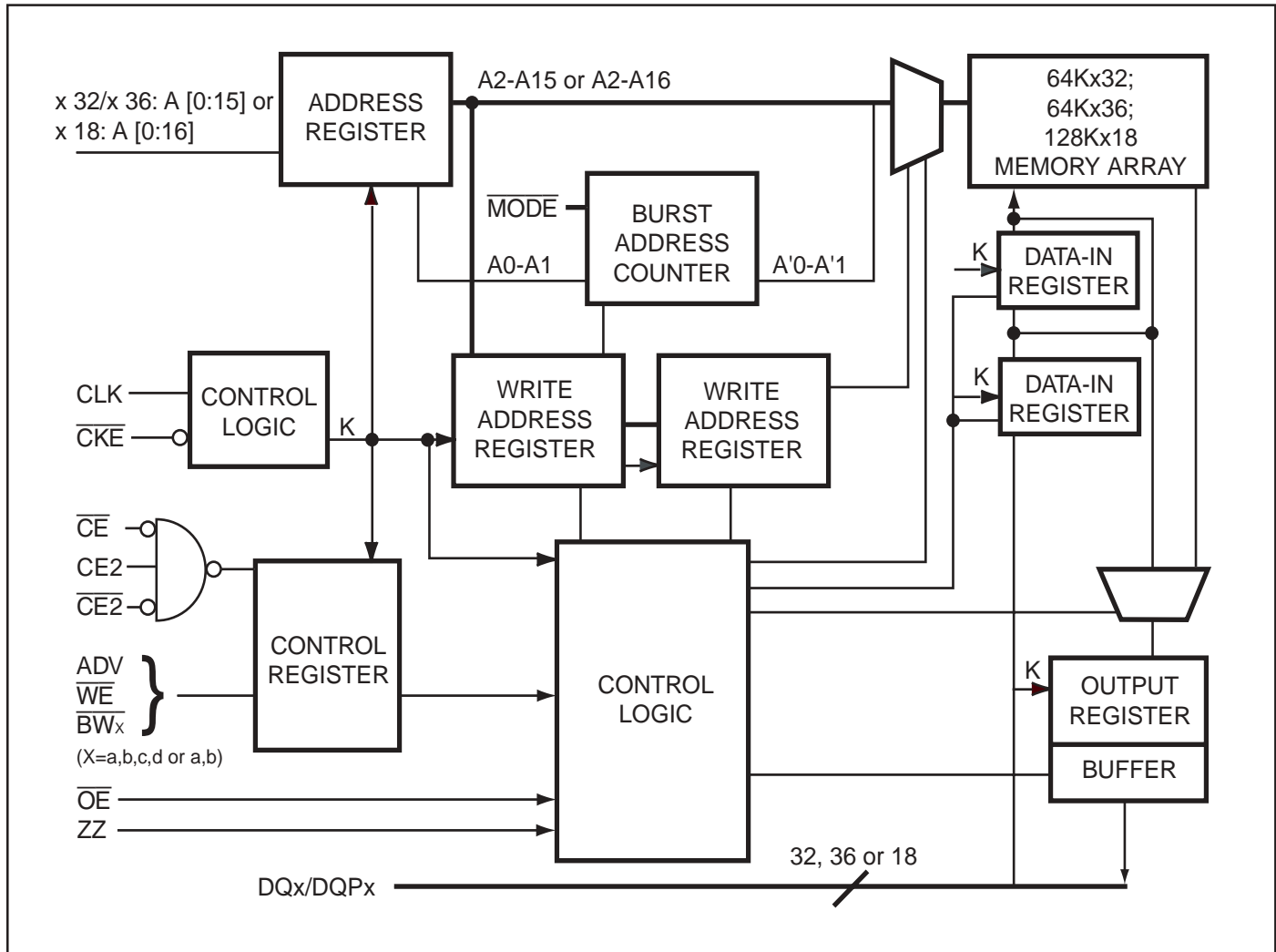
A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

FAST ACCESS TIME

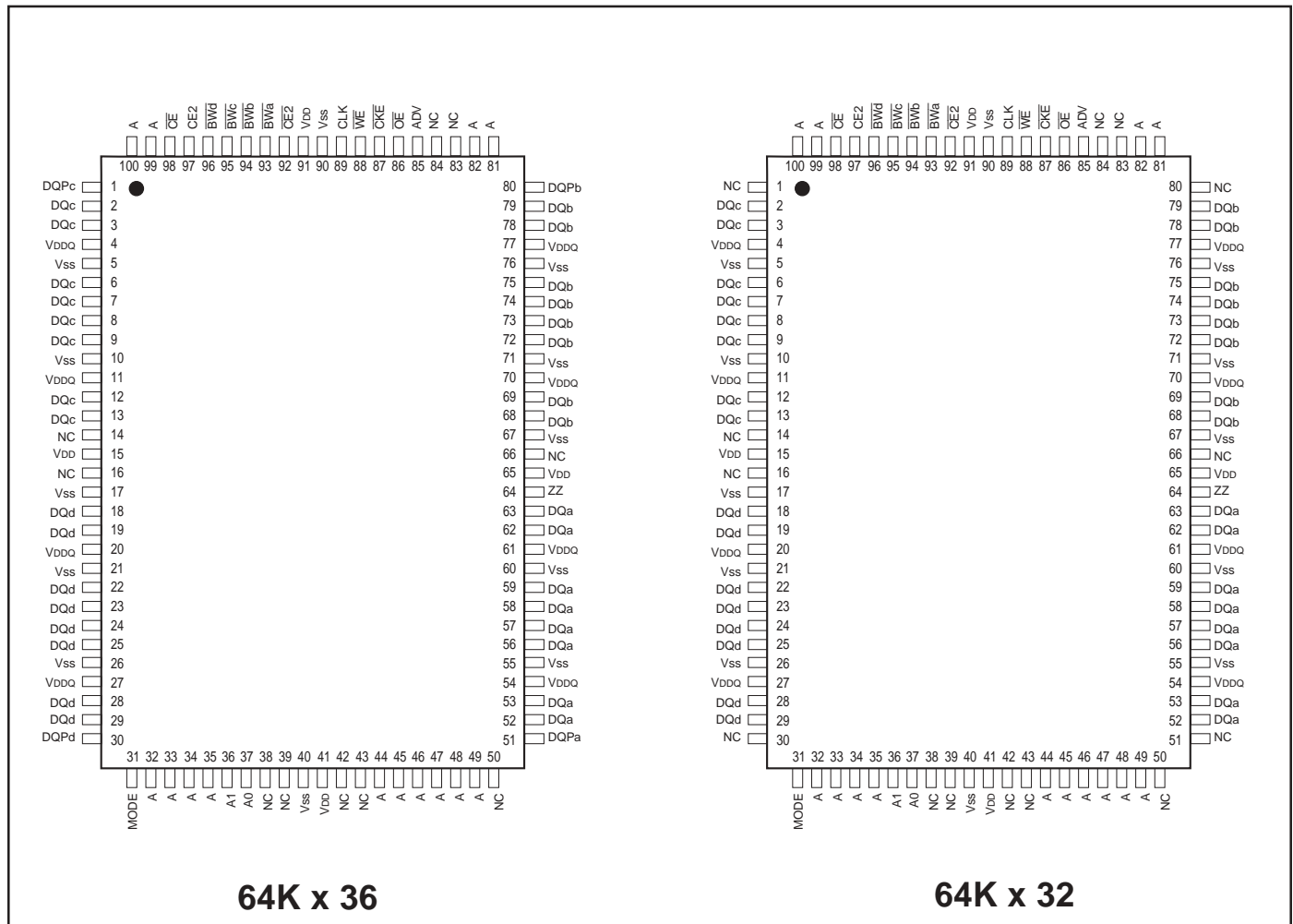
| Symbol | Parameter | -250 | -200 | Units |
|--------|-------------------|------|------|-------|
| tkQ | Clock Access Time | 2.6 | 3.1 | ns |
| tkC | Cycle Time | 4 | 5 | ns |
| | Frequency | 250 | 200 | MHz |

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BLOCK DIAGRAM



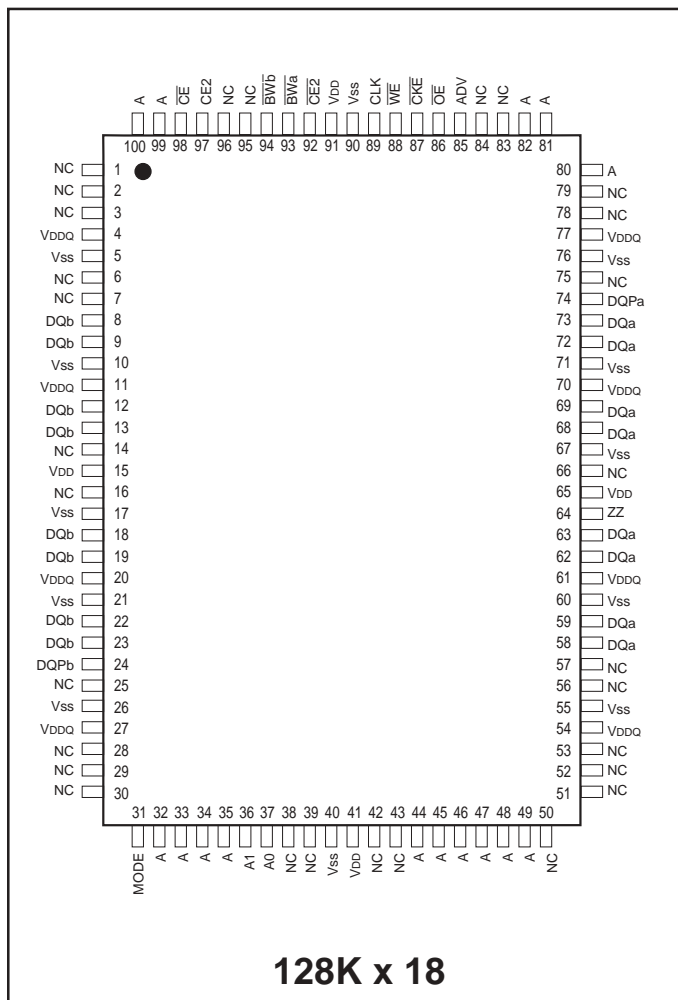
PIN CONFIGURATION
100-Pin TQFP



PIN DESCRIPTIONS

| | | | | |
|-------------------------------------|---|--|---|---|
| A0, A1 | Synchronous Address Inputs. These pins must be tied to the two LSBs of the address bus. | | \overline{CE} , CE2, $\overline{CE2}$ | Synchronous Chip Enable |
| A | Synchronous Address Inputs | | \overline{OE} | Output Enable |
| CLK | Synchronous Clock | | DQa-DQd | Synchronous Data Input/Output |
| ADV | Synchronous Burst Address Advance | | DQPa-DQPd | Parity Data I/O |
| \overline{BWa} - \overline{BWd} | Synchronous Byte Write Enable | | MODE | Burst Sequence Selection |
| \overline{WE} | Write Enable | | V _{DD} | +3.3V/2.5V Power Supply |
| \overline{CKE} | Clock Enable | | V _{SS} | Ground for output Buffer |
| V _{SS} | Ground for Core | | V _{DDQ} | Isolated Output Buffer Supply: +3.3V/2.5V |
| NC | Not Connected | | ZZ | Snooze Enable |

PIN CONFIGURATION
100-Pin TQFP

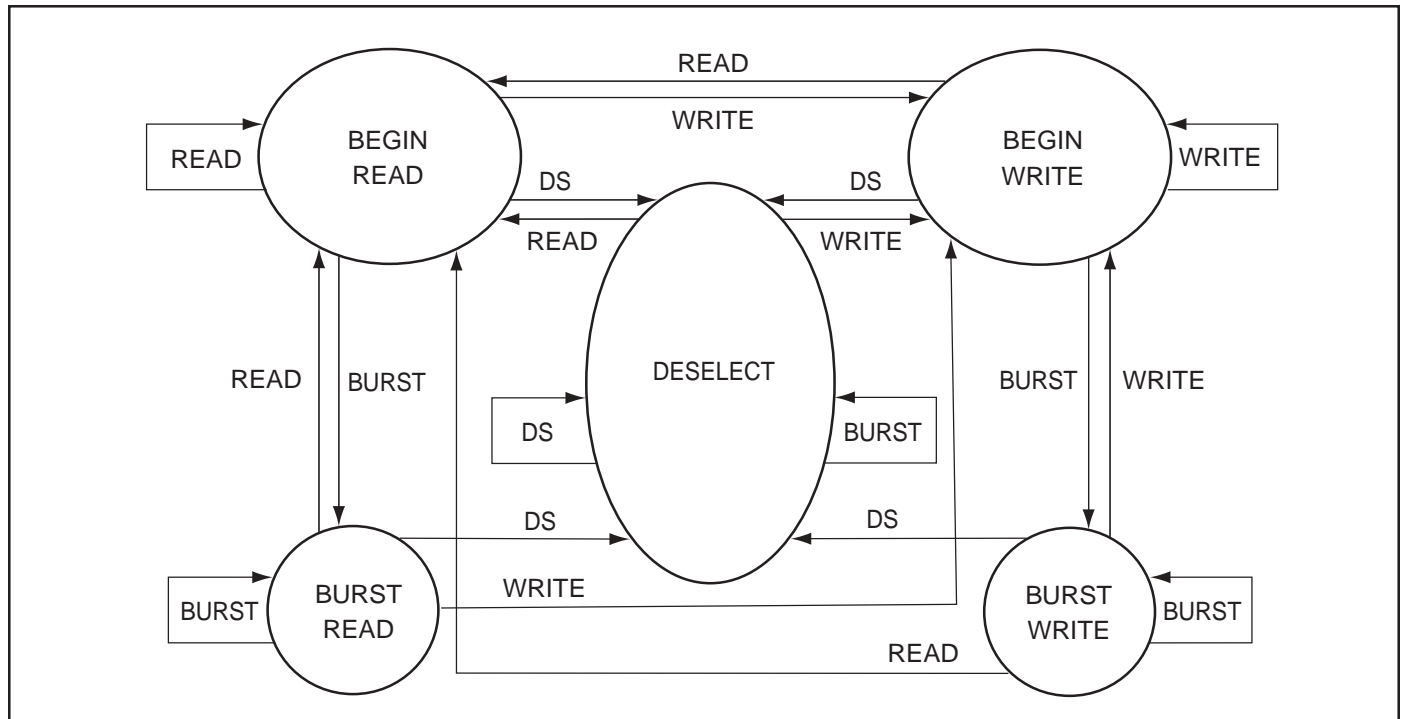


PIN DESCRIPTIONS

| | |
|-------------------------------------|--|
| A0, A1 | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A | Synchronous Address Inputs |
| CLK | Synchronous Clock |
| ADV | Synchronous Burst Address Advance |
| \overline{BWA} - \overline{BWD} | Synchronous Byte Write Enable |
| \overline{WE} | Write Enable |
| \overline{CKE} | Clock Enable |
| Vss | Ground for Core |
| NC | Not Connected |

| | |
|---|---|
| \overline{CE} , CE2, $\overline{CE2}$ | Synchronous Chip Enable |
| \overline{OE} | Output Enable |
| DQa-DQd | Synchronous Data Input/Output |
| DQPa-DQPd | Parity Data I/O |
| MODE | Burst Sequence Selection |
| VDD | +3.3V/2.5V Power Supply |
| Vss | Ground for output Buffer |
| VDDQ | Isolated Output Buffer Supply: +3.3V/2.5V |
| ZZ | Snooze Enable |

STATE DIAGRAM



SYNCHRONOUS TRUTH TABLE⁽¹⁾

| Operation | Address Used | \overline{CE} | CE2 | $\overline{CE2}$ | ADV | \overline{WE} | $\overline{BW_x}$ | \overline{OE} | \overline{CKE} | CLK |
|-----------------------|------------------|-----------------|-----|------------------|-----|-----------------|-------------------|-----------------|------------------|-----|
| Not Selected | N/A | H | X | X | L | X | X | X | L | ↑ |
| Not Selected | N/A | X | L | X | L | X | X | X | L | ↑ |
| Not Selected | N/A | X | X | H | L | X | X | X | L | ↑ |
| Not Selected Continue | N/A | X | X | X | H | X | X | X | L | ↑ |
| Begin Burst Read | External Address | L | H | L | L | H | X | L | L | ↑ |
| Continue Burst Read | Next Address | X | X | X | H | X | X | L | L | ↑ |
| NOP/Dummy Read | External Address | L | H | L | L | H | X | H | L | ↑ |
| Dummy Read | Next Address | X | X | X | H | X | X | H | L | ↑ |
| Begin Burst Write | External Address | L | H | L | L | L | L | X | L | ↑ |
| Continue Burst Write | Next Address | X | X | X | H | X | L | X | L | ↑ |
| NOP/Write Abort | N/A | L | H | L | L | L | H | X | L | ↑ |
| Write Abort | Next Address | X | X | X | H | X | H | X | L | ↑ |
| Ignore Clock | Current Address | X | X | X | X | X | X | X | H | ↑ |

Notes:

- "X" means don't care.
- The rising edge of clock is symbolized by ↑
- A continue deselect cycle can only be entered if a deselect cycle is executed first.
- $\overline{WE} = L$ means Write operation in Write Truth Table.
 $\overline{WE} = H$ means Read operation in Write Truth Table.
- Operation finally depends on status of asynchronous pins (\overline{ZZ} and \overline{OE}).

ASYNCHRONOUS TRUTH TABLE⁽¹⁾

| Operation | ZZ | \overline{OE} | I/O STATUS |
|------------|----|-----------------|-------------|
| Sleep Mode | H | X | High-Z |
| Read | L | L | DQ |
| | L | H | High-Z |
| Write | L | X | Din, High-Z |
| Deselected | L | X | High-Z |

Notes:

1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

WRITE TRUTH TABLE (x18)

| Operation | \overline{WE} | \overline{BW}_a | \overline{BW}_b |
|-----------------|-----------------|-------------------|-------------------|
| READ | H | X | X |
| WRITE BYTE a | L | L | H |
| WRITE BYTE b | L | H | L |
| WRITE ALL BYTES | L | L | L |
| WRITE ABORT/NOP | L | H | H |

Notes:

1. X means "Don't Care".
2. All inputs in this table must be setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x32/x36)

| Operation | WE | BW_a | BW_b | BW_c | BW_d |
|-----------------|-----------|-----------------------|-----------------------|-----------------------|-----------------------|
| READ | H | X | X | X | X |
| WRITE BYTE a | L | L | H | H | H |
| WRITE BYTE b | L | H | L | H | H |
| WRITE BYTE c | L | H | H | L | H |
| WRITE BYTE d | L | H | H | H | L |
| WRITE ALL BYTES | L | L | L | L | L |
| WRITE ABORT/NOP | L | H | H | H | H |

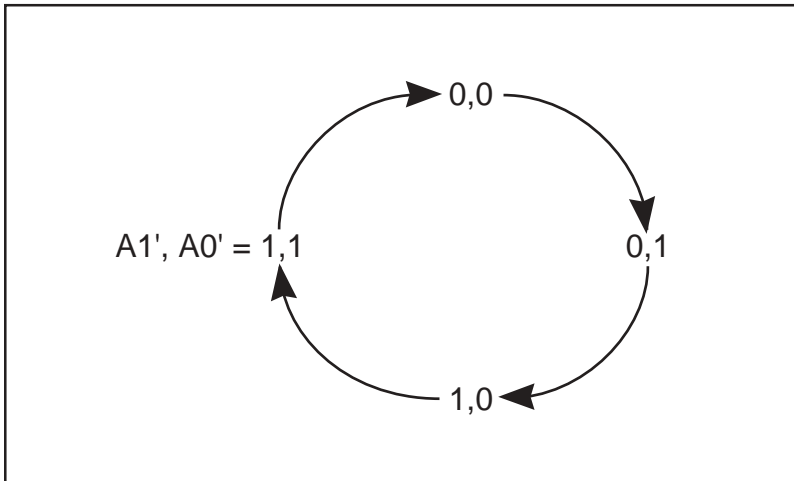
Notes:

1. X means "Don't Care".
2. All inputs in this table must be set up and hold time around the rising edge of CLK.

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or NC)

| External Address A1 A0 | 1st Burst Address A1 A0 | 2nd Burst Address A1 A0 | 3rd Burst Address A1 A0 |
|---------------------------|----------------------------|----------------------------|----------------------------|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

LINEAR BURST ADDRESS TABLE (MODE = V_{SS})



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|------------------------------------|--|--------------------------------|------|
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _D | Power Dissipation | 1.6 | W |
| I _{OUT} | Output Current (per I/O) | 100 | mA |
| V _{IN} , V _{OUT} | Voltage Relative to V _{SS} for I/O Pins | -0.5 to V _{DDQ} + 0.3 | V |
| V _{IN} | Voltage Relative to V _{SS} for Address and Control Inputs | -0.3 to 4.6 | V |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61NLPx)

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|---------------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |
| Industrial | -40°C to +85°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |

OPERATING RANGE (IS61NVPx)

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|---------------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 2.5V ± 5% | 2.5V ± 5% |
| Industrial | -40°C to +85°C | 2.5V ± 5% | 2.5V ± 5% |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | 3.3V | | 2.5V | | Unit |
|-----------------|------------------------|--|------|-----------------------|------|-----------------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | I _{OH} = -4.0 mA (3.3V) I _{OH} = -1.0 mA (2.5V) | 2.4 | — | 2.0 | — | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 8.0 mA (3.3V) I _{OL} = 1.0 mA (2.5V) | — | 0.4 | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | V _{DD} + 0.3 | 1.7 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW Voltage | | -0.3 | 0.8 | -0.3 | 0.7 | V |
| I _{LI} | Input Leakage Current | V _{SS} ≤ V _{IN} ≤ V _{DD} ⁽¹⁾ | -5 | 5 | -5 | 5 | μA |
| I _{LO} | Output Leakage Current | V _{SS} ≤ V _{OUT} ≤ V _{DDQ} , $\overline{OE} = V_{IH}$ | -5 | 5 | -5 | 5 | μA |

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | Temp. range | -250 MAX | | -200 MAX | | Unit |
|------------------|--------------------------------|--|-------------------------------------|----------------|------------|----------------|------------|------|
| | | | | x18 | x32/x36 | x18 | x32/x36 | |
| I _{CC} | AC Operating Supply Current | Device Selected, $\overline{OE} = V_{IH}$, ZZ ≤ V _{IL} , All Inputs ≤ 0.2V or ≥ V _{DD} - 0.2V, Cycle Time ≥ t _{kc} min. | Com. Ind. | 225 250 | 225 250 | 200 210 | 200 210 | mA |
| I _{SB} | Standby Current TTL Input | Device Deselected, V _{DD} = Max., All Inputs ≤ V _{IL} or ≥ V _{IH} , ZZ ≤ V _{IL} , f = Max. | Com. Ind. | 90 100 | 90 100 | 90 100 | 90 100 | mA |
| I _{SBI} | Standby Current CMOS Input | Device Deselected, V _{DD} = Max., V _{IN} ≤ V _{SS} + 0.2V or ≥ V _{DD} - 0.2V f = 0 | Com. Ind. typ. ⁽²⁾ | 70 75 40 | 70 75 | 70 75 40 | 70 75 | mA |
| I _{SB2} | Sleep Mode | ZZ > V _{IH} | Com. Ind. typ. ⁽²⁾ | 30 35 20 | 30 35 | 30 35 20 | 30 35 | mA |

Note:

1. MODE pin has an internal pullup and should be tied to V_{DD} or V_{SS}. It exhibits ±100μA maximum leakage current when tied to ≤ V_{SS} + 0.2V or ≥ V_{DD} - 0.2V.
2. Typical values are measured at V_{DD} = 3.3V, T_A = 25°C and not 100% tested.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{OUT} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

3.3V I/O OUTPUT LOAD EQUIVALENT

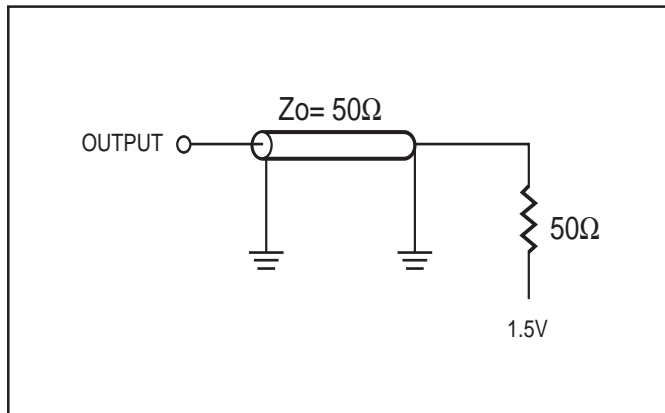


Figure 1

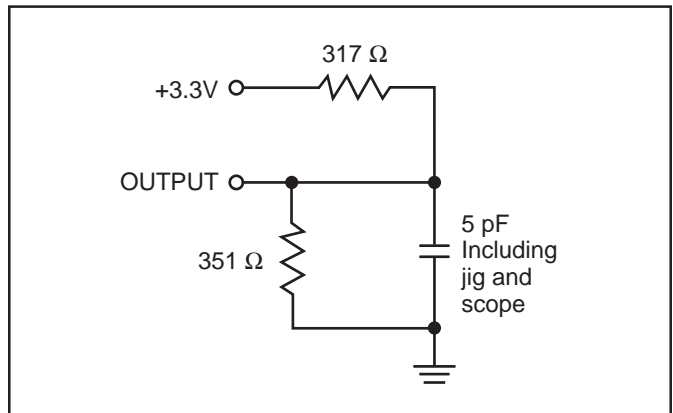


Figure 2

2.5V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 2.5V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.25V |
| Output Load | See Figures 3 and 4 |

2.5V I/O OUTPUT LOAD EQUIVALENT

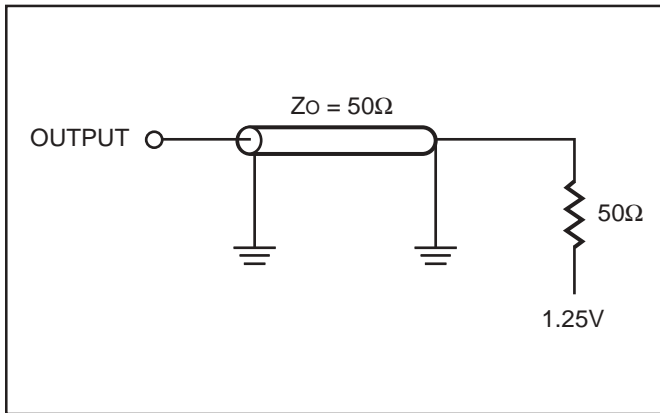


Figure 3

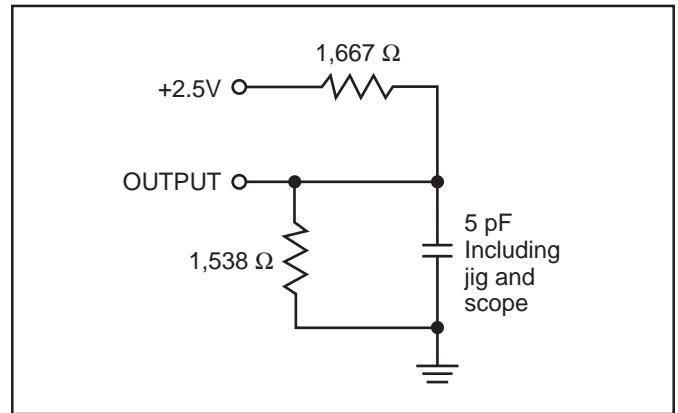


Figure 4

READ/WRITE CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | -250 | | -200 | | Unit |
|-----------------------------------|---------------------------------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| fmax | Clock Frequency | — | 250 | — | 200 | MHz |
| t _{κC} | Cycle Time | 4.0 | — | 5 | — | ns |
| t _{κH} | Clock High Time | 1.7 | — | 2 | — | ns |
| t _{κL} | Clock Low Time | 1.7 | — | 2 | — | ns |
| t _{κQ} | Clock Access Time | — | 2.6 | — | 3.1 | ns |
| t _{κQX⁽²⁾} | Clock High to Output Invalid | 0.8 | — | 1.5 | — | ns |
| t _{κQLZ^(2,3)} | Clock High to Output Low-Z | 0.8 | — | 1 | — | ns |
| t _{κQHZ^(2,3)} | Clock High to Output High-Z | — | 2.6 | — | 3.0 | ns |
| t _{OEQ} | Output Enable to Output Valid | — | 2.8 | — | 3.1 | ns |
| t _{OE^(2,3)} | Output Enable to Output Low-Z | 0 | — | 0 | — | ns |
| t _{OE^(2,3)} | Output Disable to Output High-Z | — | 2.6 | — | 3.0 | ns |
| t _{AS} | Address Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{WS} | Read/Write Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{CES} | Chip Enable Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{SE} | Clock Enable Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{ADVS} | Address Advance Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{DS} | Data Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{AH} | Address Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{HE} | Clock Enable Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{WH} | Write Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{CEH} | Chip Enable Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{ADVH} | Address Advance Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{DH} | Data Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{PDS} | ZZ High to Power Down | — | 2 | — | 2 | cyc |
| t _{PUS} | ZZ Low to Power Down | — | 2 | — | 2 | cyc |

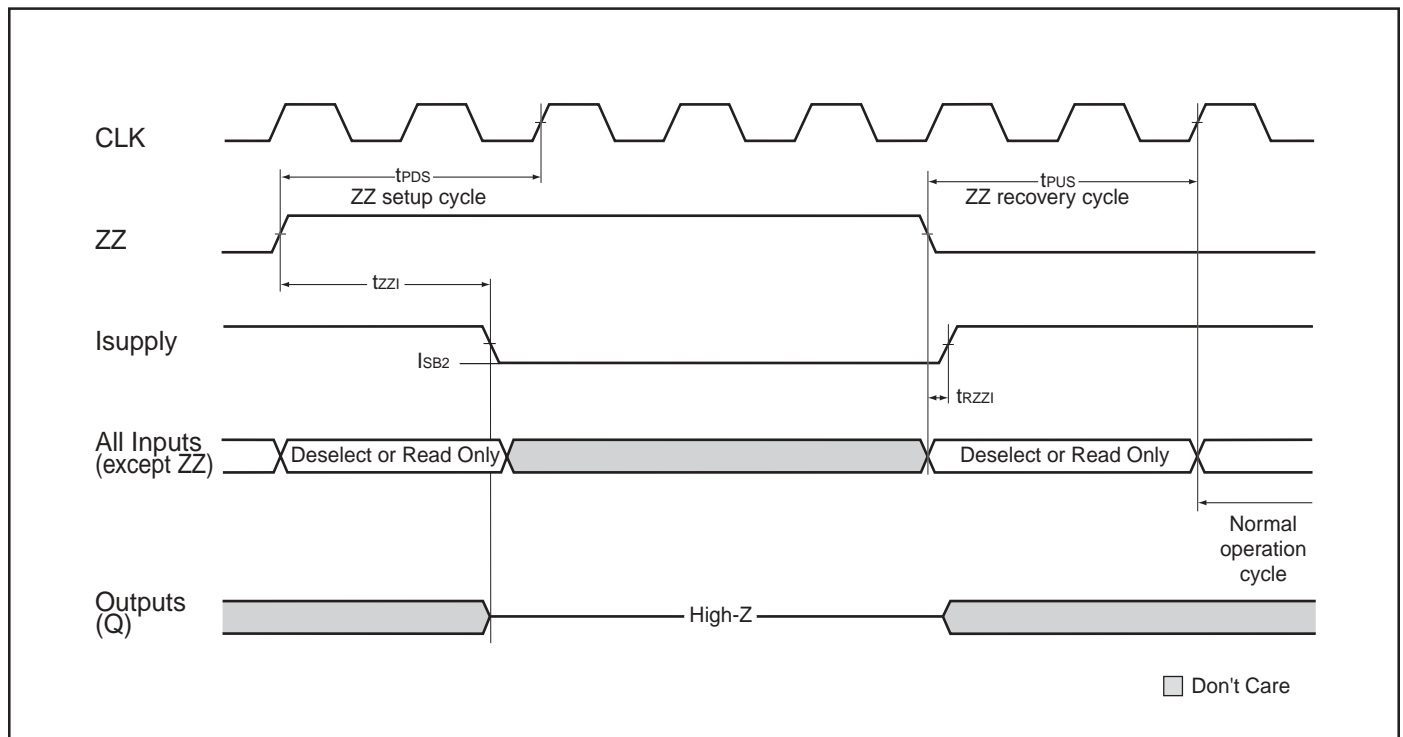
Notes:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

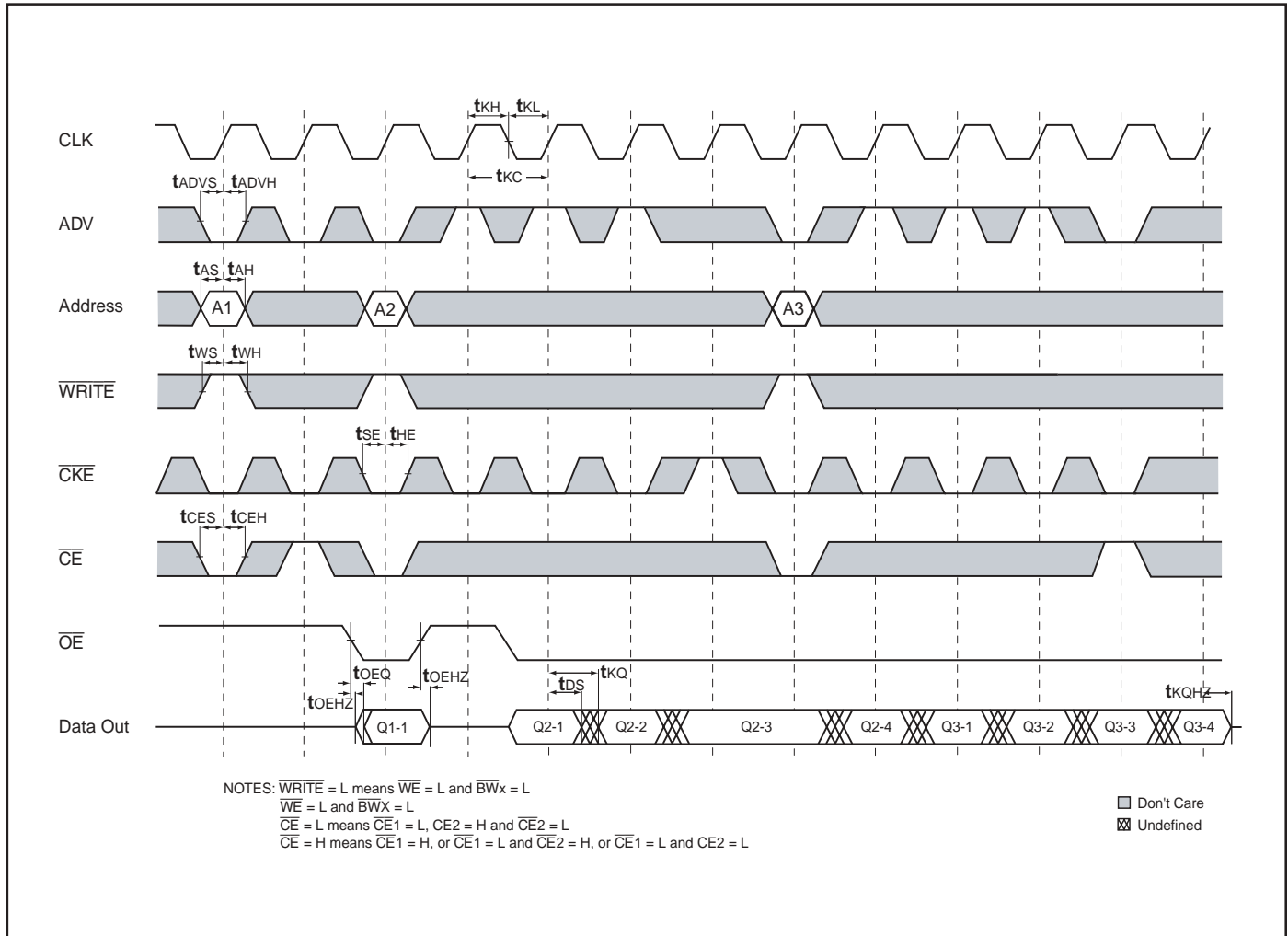
SLEEP MODE ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|-------------------|-----------------------------------|----------------------|------|------|-------|
| I _{SB2} | Current during SLEEP MODE | ZZ ≥ V _{IH} | | 35 | mA |
| t _{PDS} | ZZ active to input ignored | | 2 | | cycle |
| t _{PUS} | ZZ inactive to input sampled | | 2 | | cycle |
| t _{ZZI} | ZZ active to SLEEP current | | 2 | | cycle |
| t _{TRZI} | ZZ inactive to exit SLEEP current | | 0 | | ns |

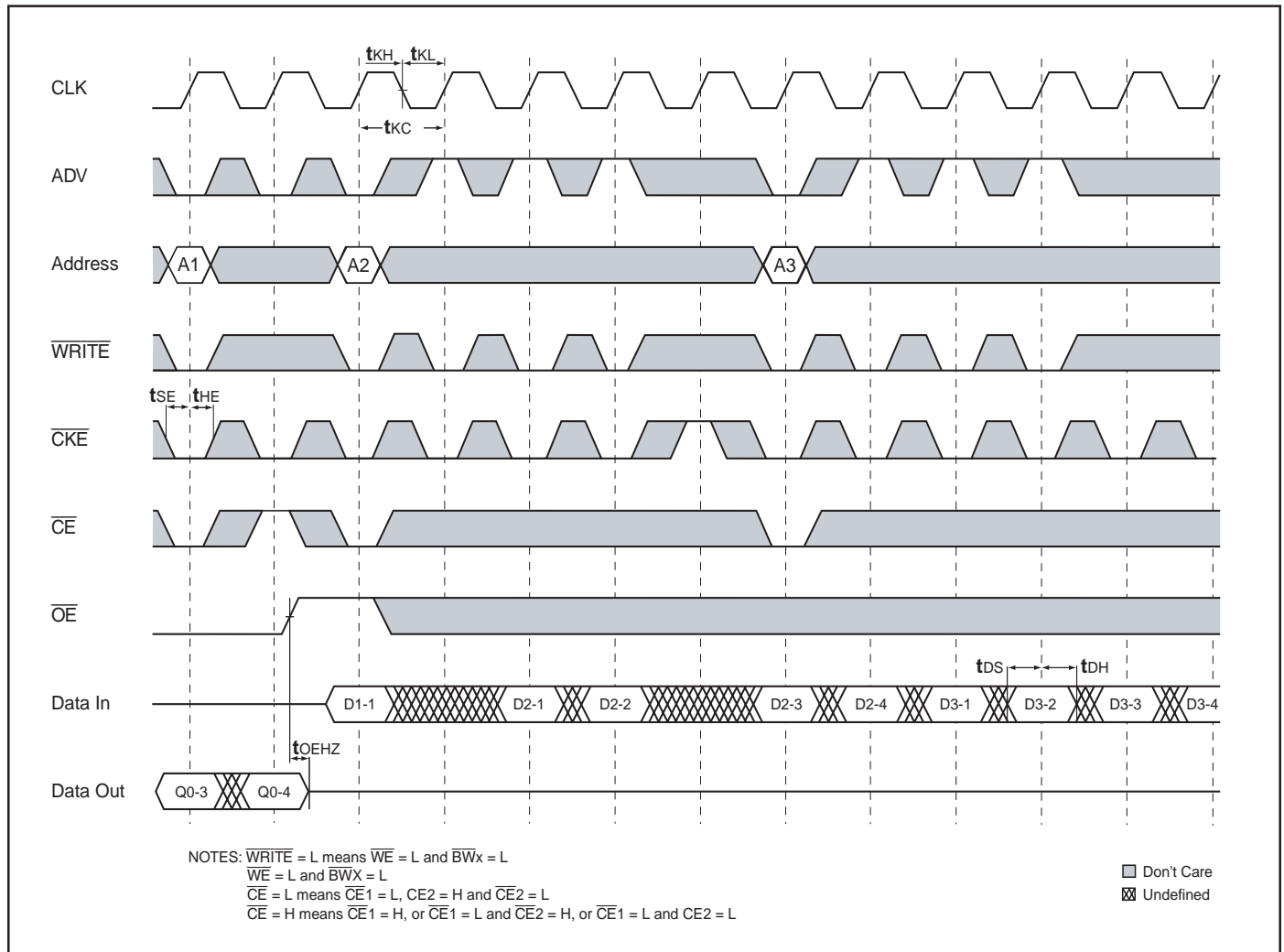
SLEEP MODE TIMING



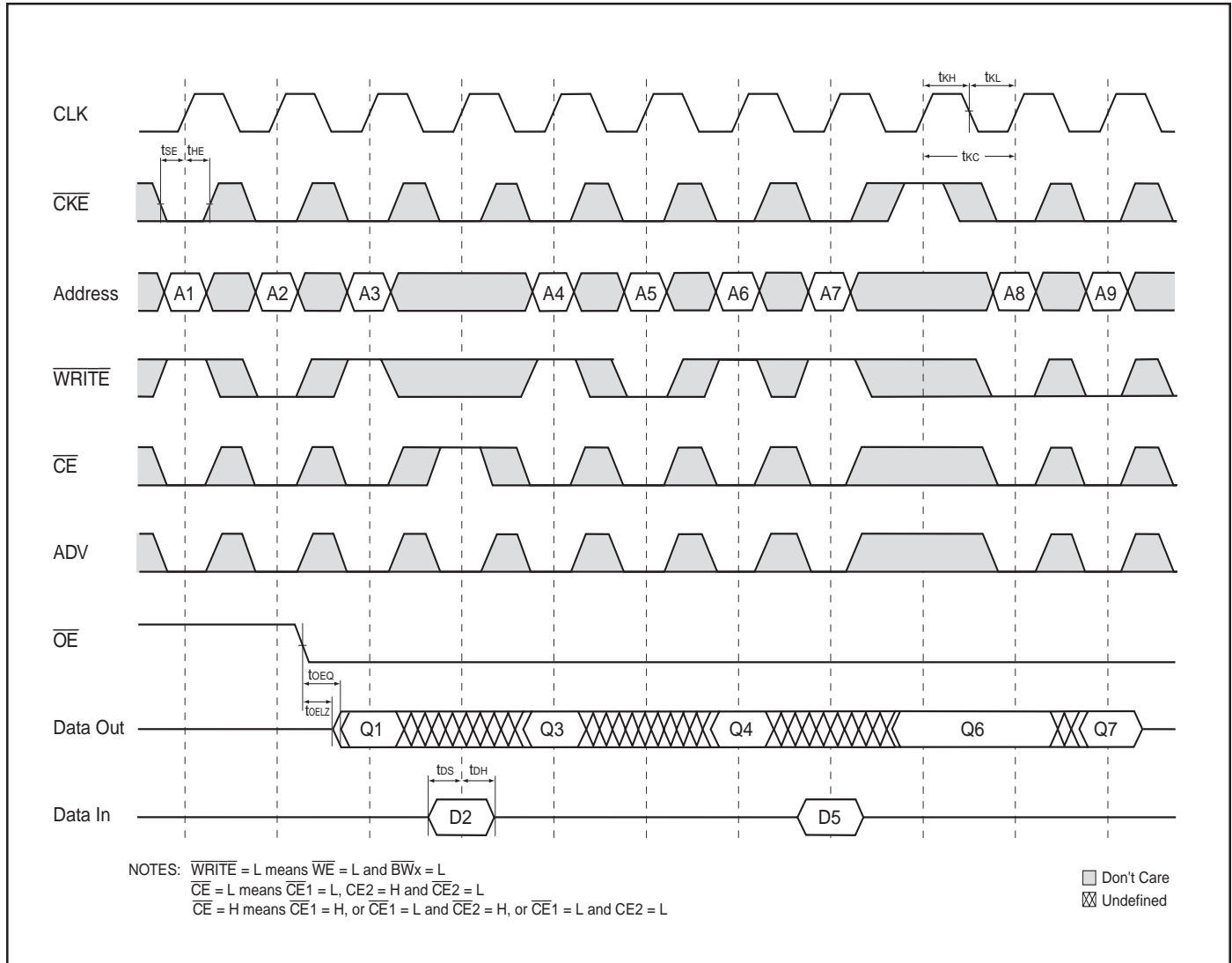
READ CYCLE TIMING



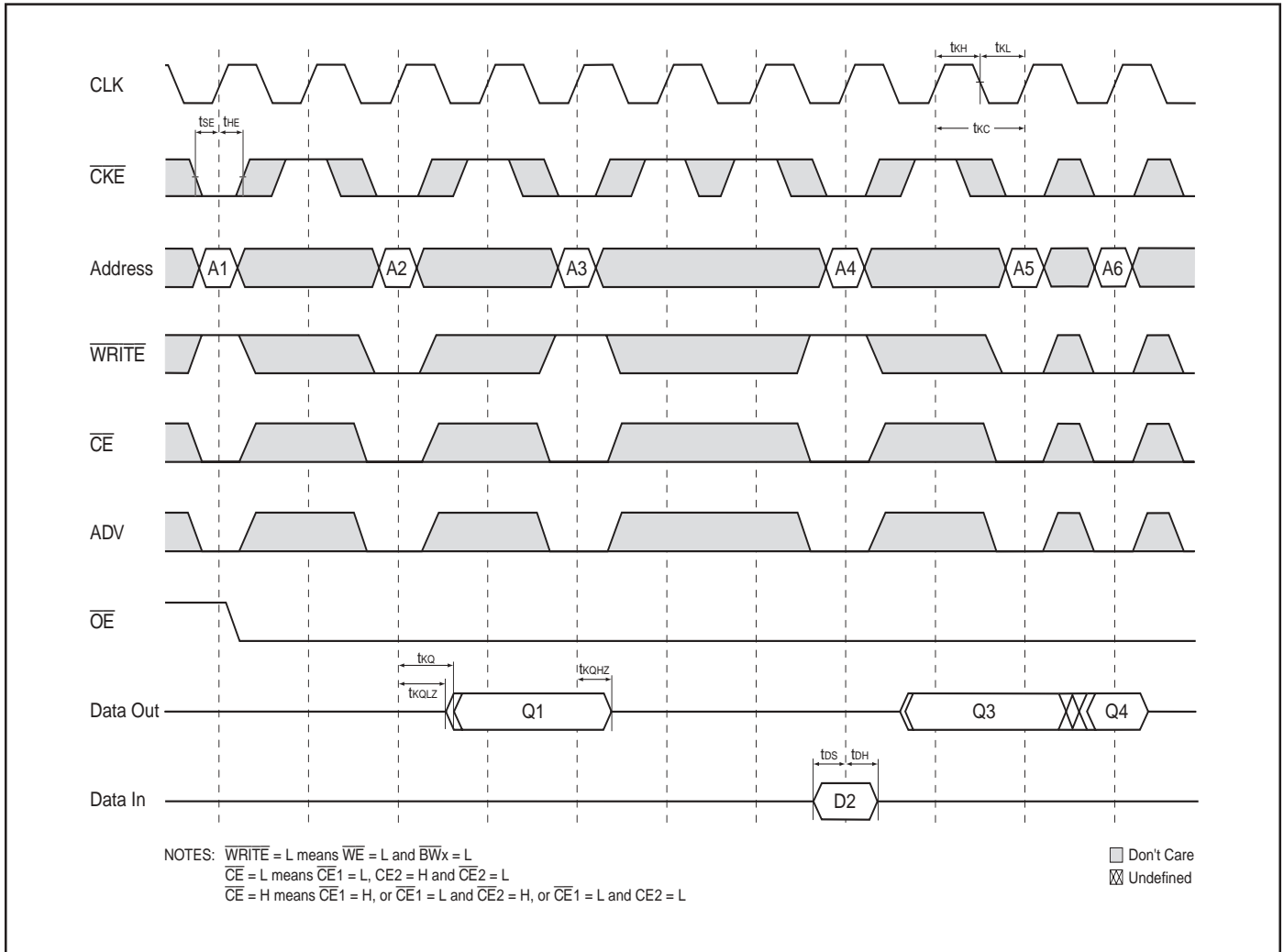
WRITE CYCLE TIMING



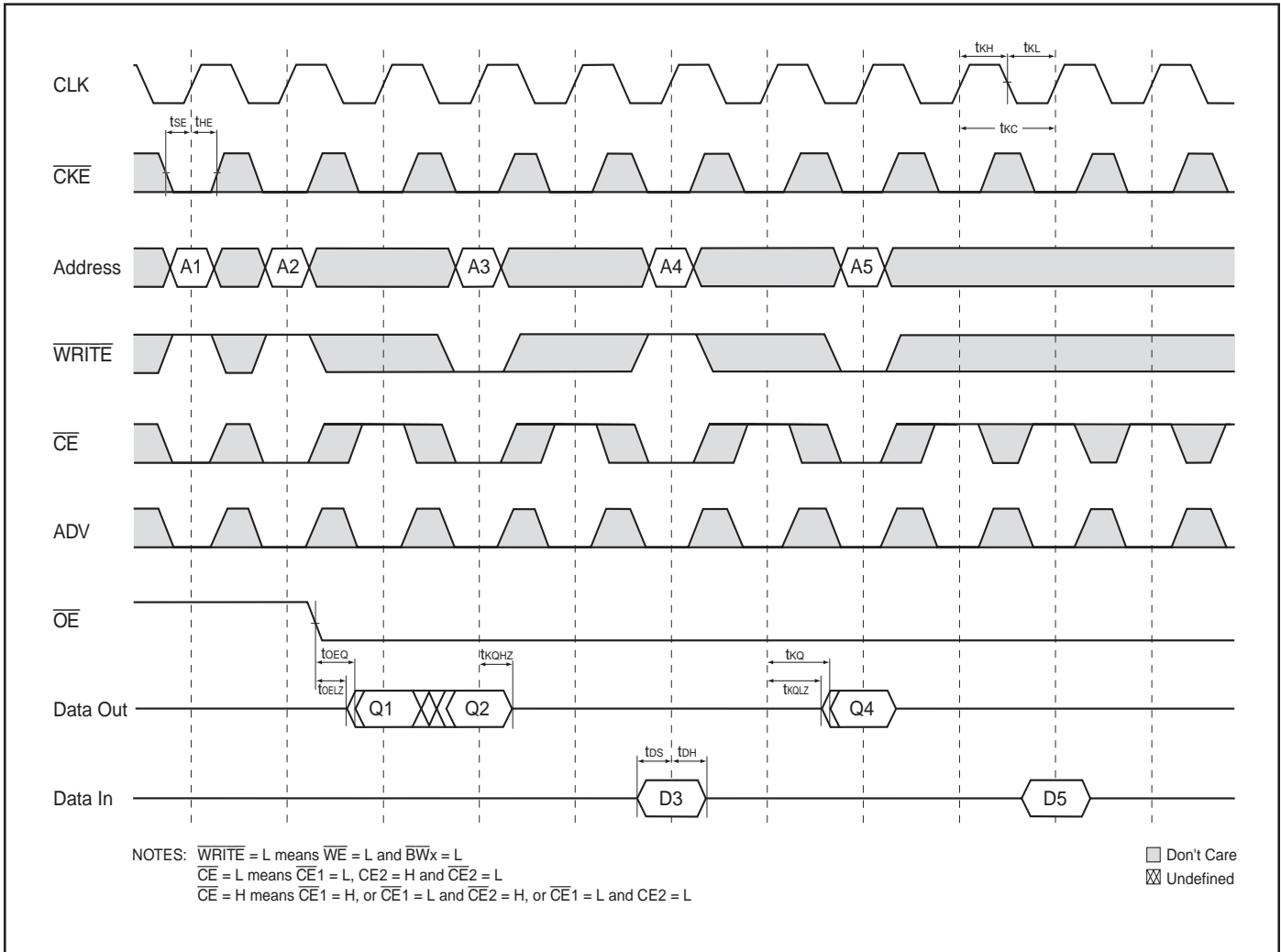
SINGLE READ/WRITE CYCLE TIMING



CKE OPERATION TIMING



CE OPERATION TIMING



ORDERING INFORMATION (V_{DD} = 3.3V/V_{DDQ} = 2.5V/3.3V)

Commercial Range: 0°C to +70°C

| Access Time | Order Part Number | Package |
|----------------|---------------------|----------|
| 64Kx32 | | |
| 250 | IS61NLP6432A-250TQ | 100 TQFP |
| 200 | IS61NLP6432A-200TQ | 100 TQFP |
| 64Kx36 | | |
| 250 | IS61NLP6436A-250TQ | 100 TQFP |
| 200 | IS61NLP6436A-200TQ | 100 TQFP |
| 128Kx18 | | |
| 250 | IS61NLP12818A-250TQ | 100 TQFP |
| 200 | IS61NLP12818A-200TQ | 100 TQFP |

Industrial Range: -40°C to +85°C

| Access Time | Order Part Number | Package |
|----------------|-----------------------|---------------------|
| 64Kx32 | | |
| 250 | IS61NLP6432A-250TQI | 100 TQFP |
| 200 | IS61NLP6432A-200TQI | 100 TQFP |
| 200 | IS61NLP6432A-200TQLI | 100 TQFP, Lead-free |
| 64Kx36 | | |
| 250 | IS61NLP6436A-250TQI | 100 TQFP |
| 200 | IS61NLP6436A-200TQI | 100 TQFP |
| 128Kx18 | | |
| 250 | IS61NLP12818A-250TQI | 100 TQFP |
| 200 | IS61NLP12818A-200TQI | 100 TQFP |
| 200 | IS61NLP12818A-200TQLI | 100 TQFP, Lead-free |

ORDERING INFORMATION (V_{DD} = 2.5V/V_{DDQ} = 2.5V)

Commercial Range: 0°C to +70°C

| Access Time | Order Part Number | Package |
|----------------|---------------------|----------|
| 64Kx36 | | |
| 250 | IS61NVP6436A-250TQ | 100 TQFP |
| 200 | IS61NVP6436A-200TQ | 100 TQFP |
| 128Kx18 | | |
| 250 | IS61NVP12818A-250TQ | 100 TQFP |
| 200 | IS61NVP12818A-200TQ | 100 TQFP |

Industrial Range: -40°C to +85°C

| Access Time | Order Part Number | Package |
|----------------|----------------------|----------|
| 64Kx36 | | |
| 250 | IS61NVP6436A-250TQI | 100 TQFP |
| 200 | IS61NVP6436A-200TQI | 100 TQFP |
| 128Kx18 | | |
| 250 | IS61NVP12818A-250TQI | 100 TQFP |
| 200 | IS61NVP12818A-200TQI | 100 TQFP |

PACKAGING INFORMATION

TQFP (Thin Quad Flat Pack Package)

Package Code: TQ



Thin Quad Flat Pack (TQ)

| Symbol | Millimeters | | Inches | | Symbol | Millimeters | | Inches | |
|---------------|-------------|-------|------------|-------|-----------|-------------|------------|--------|-----|
| | Min | Max | Min | Max | | Min | Max | Min | Max |
| Ref. Std. | | | | | | | | | |
| No. Leads (N) | 100 | | | | 128 | | | | |
| A | — | 1.60 | — | 0.063 | — | 1.60 | — | 0.063 | |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 | 0.05 | 0.15 | 0.002 | 0.006 | |
| A2 | 1.35 | 1.45 | 0.053 | 0.057 | 1.35 | 1.45 | 0.053 | 0.057 | |
| b | 0.22 | 0.38 | 0.009 | 0.015 | 0.17 | 0.27 | 0.007 | 0.011 | |
| D | 21.90 | 22.10 | 0.862 | 0.870 | 21.80 | 22.20 | 0.858 | 0.874 | |
| D1 | 19.90 | 20.10 | 0.783 | 0.791 | 19.90 | 20.10 | 0.783 | 0.791 | |
| E | 15.90 | 16.10 | 0.626 | 0.634 | 15.80 | 16.20 | 0.622 | 0.638 | |
| E1 | 13.90 | 14.10 | 0.547 | 0.555 | 13.90 | 14.10 | 0.547 | 0.555 | |
| e | 0.65 BSC | | 0.026 BSC | | 0.50 BSC | | 0.020 BSC | | |
| L | 0.45 | 0.75 | 0.018 | 0.030 | 0.45 | 0.75 | 0.018 | 0.030 | |
| L1 | 1.00 REF. | | 0.039 REF. | | 1.00 REF. | | 0.039 REF. | | |
| C | 0° | 7° | 0° | 7° | 0° | 7° | 0° | 7° | |

Notes:

1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
3. Controlling dimension: millimeters.